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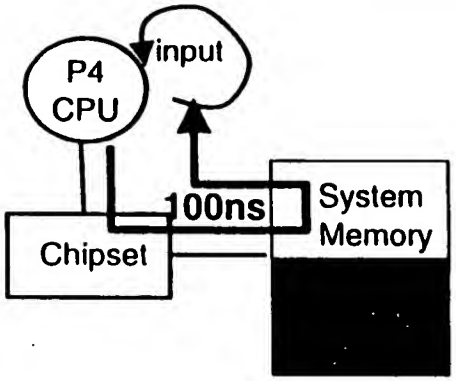
Figure 1(a)
(Prior Art)

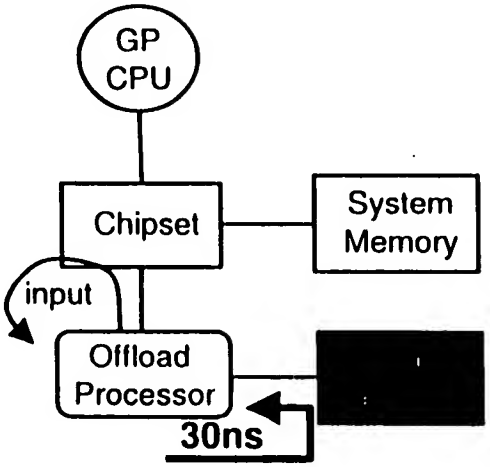
Properties of DFA and NFA techniques used on conventional microprocessors	**Storage: Bound on # of States (for an R character Regular Expression)**	**Evaluation time (for N bytes of Input) [order of]**
Deterministic Finite State Automata or DFA running on a GP CPU	**2^R** (needs very large memory)	**N** memory access cycles
Non-Deterministic Finite State Automata or NFA running on a GP CPU	**R**	**R * N** cpu cache+branch cycles

Figure 1(b)
(Prior Art)

CPU walking DFA table in DRAM



Coprocessor closer to table in SRAM



Performance on evaluating Regular Expressions on every byte of input stream

1000s of REs @ 100 Mbps	100s of REs @ 280 Mbps
Gigabytes of Memory	100s of MBs of SRAM

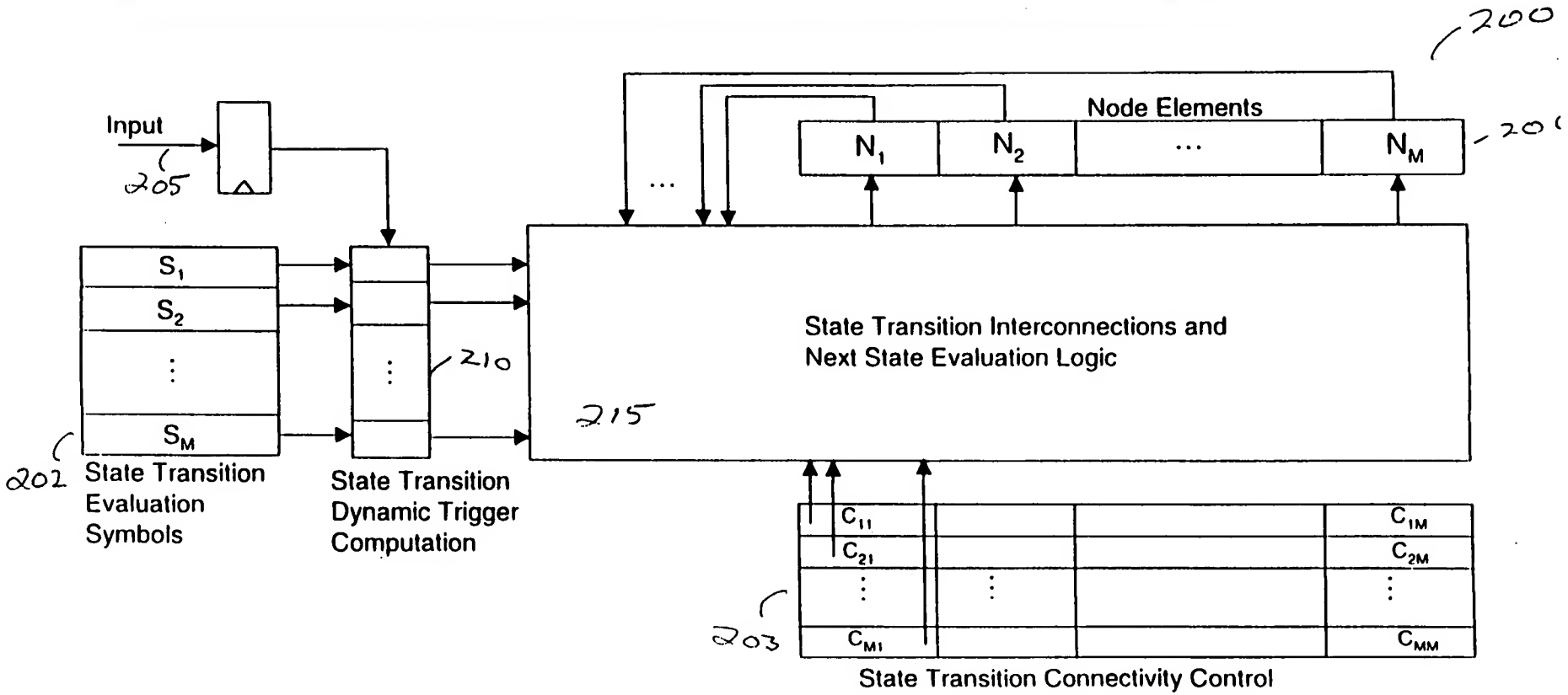

200
Input
205
Node Elements
N_1
N_2
...
N_M
201
...
S_1
S_2
S_M
210
State Transition Interconnections and
Next State Evaluation Logic
215
202
State Transition
Evaluation
Symbols
State Transition
Dynamic Trigger
Computation
C_{11}
C_{1M}
C_{21}
C_{2M}
C_{M1}
C_{MM}
203
State Transition Connectivity Control

Fig. 2

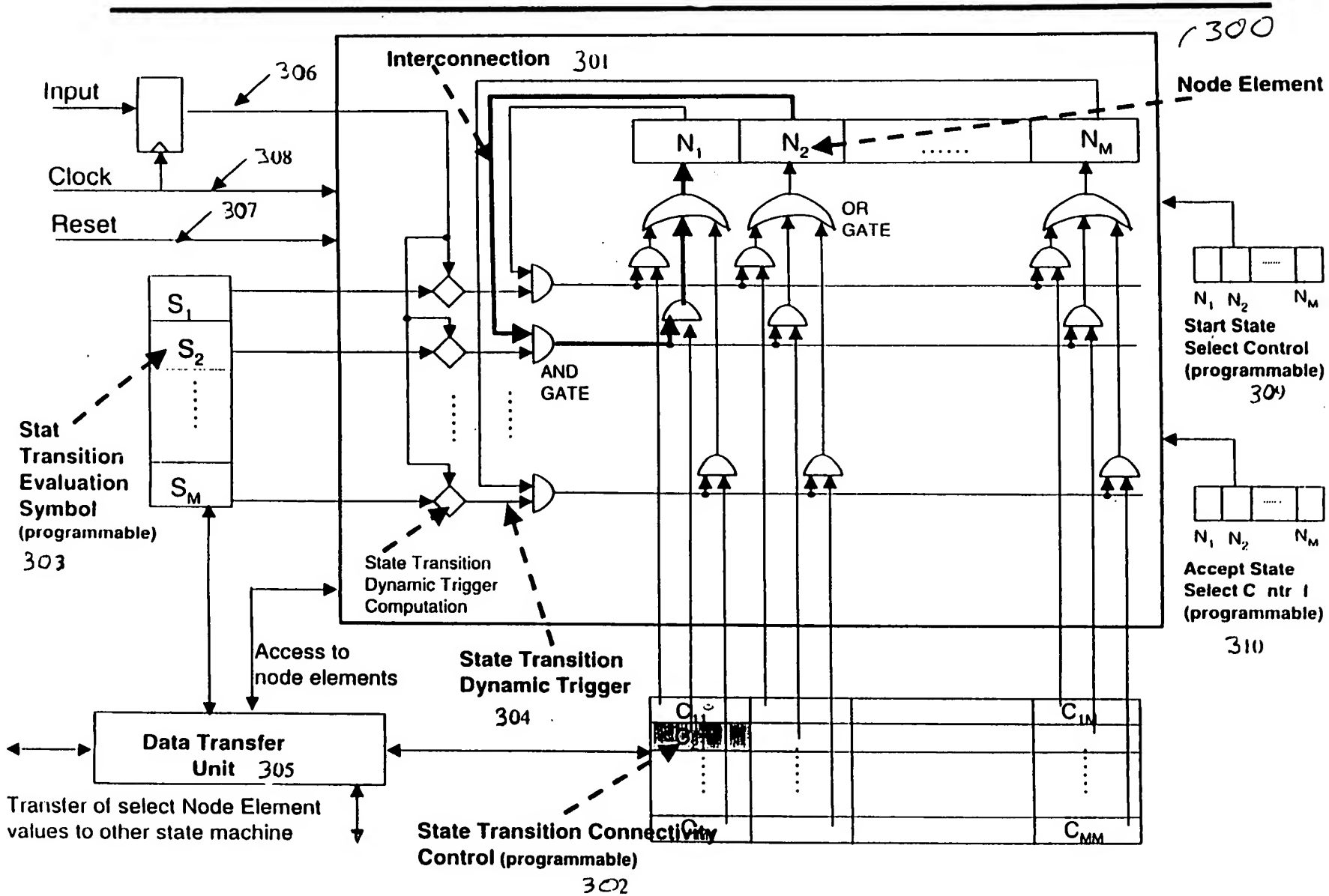

300
Interconnection 301
Node Element
Input
306
Clock
308
Reset
307
N_1
N_2
.....
N_M
OR GATE
AND GATE
S_1
S_2
S_M
Stat Transition Evaluation Symbol (programmable)
303
N_1 N_2 N_M
Start State Select Control (programmable)
309
N_1 N_2 N_M
Accept State Select C ntr l (programmable)
310
State Transition Dynamic Trigger Computation
Access to node elements
State Transition Dynamic Trigger
304
Data Transfer Unit 305
Transfer of select Node Element values to other state machine
C_{11}
C_{1M}
C_{M1}
C_{MM}
State Transition Connectivity Control (programmable)
302

Fig. 3

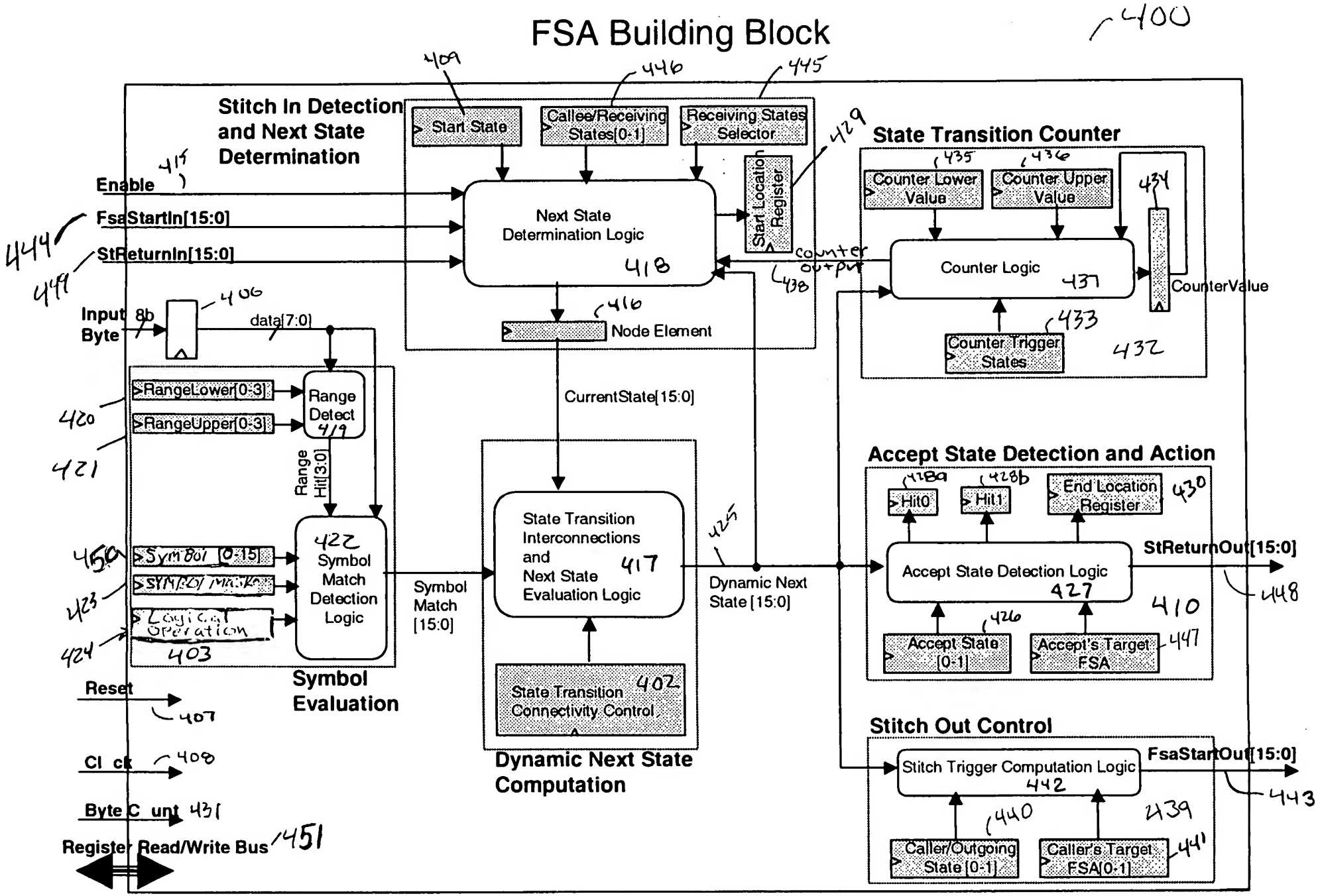

FSA Building Block
400
Stitch In Detection and Next State Determination
Start State
Callee/Receiving States[0:1]
Receiving States Selector
Start Location Register
Next State Determination Logic
418
Node Element
Enable
FsaStartIn[15:0]
StReturnIn[15:0]
Input Byte
8b
data[7:0]
RangeLower[0:3]
RangeUpper[0:3]
Range Detect
Range Hit[3:0]
Symbol[0:15]
Symbol Mask
Logical Operation
Symbol Match Detection Logic
Symbol Evaluation
CurrentState[15:0]
State Transition Interconnections and Next State Evaluation Logic
417
State Transition Connectivity Control
Dynamic Next State Computation
Symbol Match [15:0]
Dynamic Next State [15:0]
State Transition Counter
Counter Lower Value
Counter Upper Value
Counter Logic
437
Counter Trigger States
CounterValue
counter output
Accept State Detection and Action
Hit0
Hit1
End Location Register
Accept State Detection Logic
427
Accept State [0:1]
Accept's Target FSA
StReturnOut[15:0]
Stitch Out Control
Stitch Trigger Computation Logic
442
Caller/Outgoing State [0:1]
Caller's Target FSA[0:1]
FsaStartOut[15:0]
Reset
Clock
Byte Count
Register Read/Write Bus
403

Fig. 4

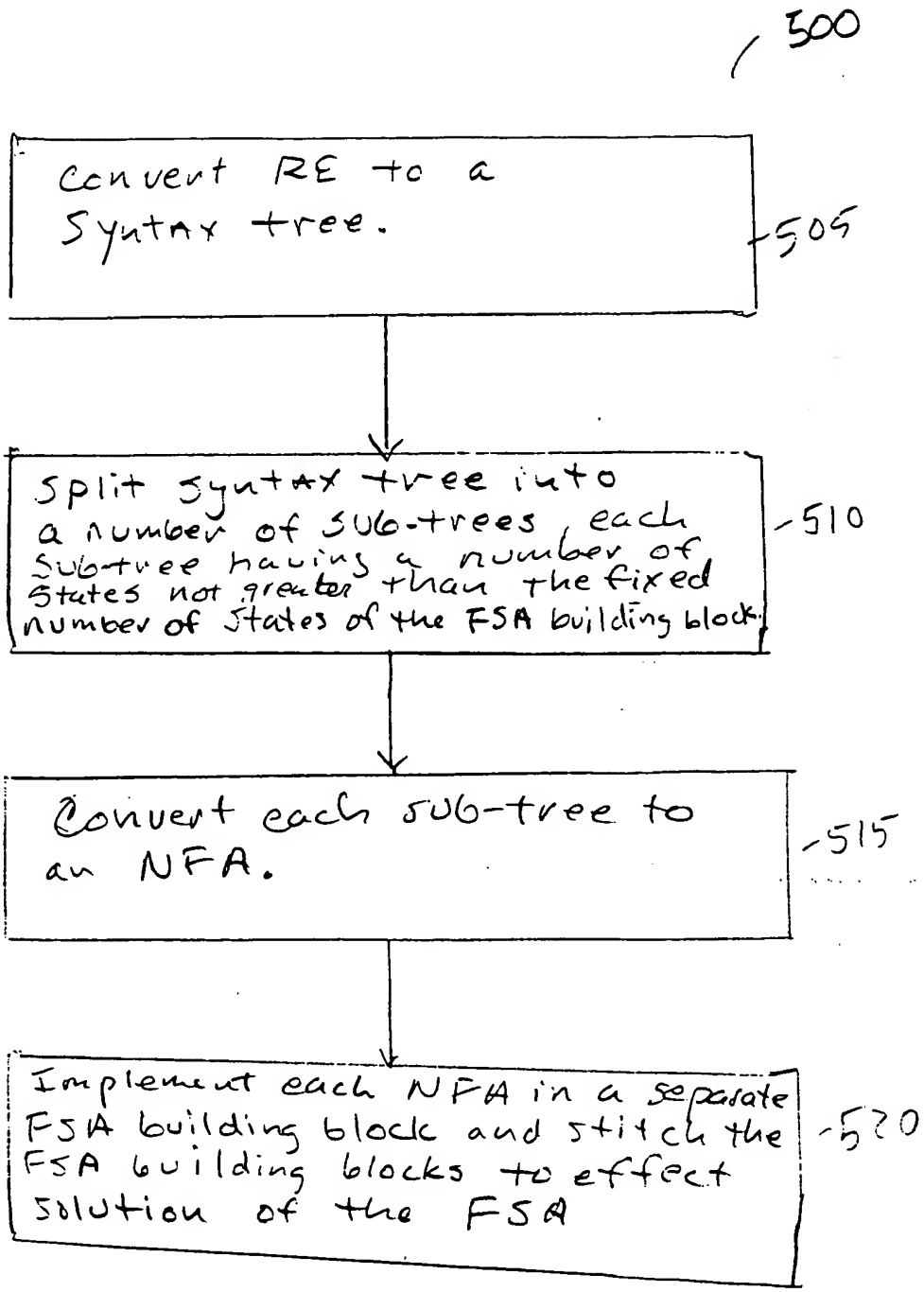

300
Convert RE to a Syntax tree.
505
Split syntax tree into a number of sub-trees, each sub-tree having a number of states not greater than the fixed number of states of the FSA building block.
510
Convert each sub-tree to an NFA.
515
Implement each NFA in a separate FSA building block and stitch the FSA building blocks to effect solution of the FSA
520

Fig. 5

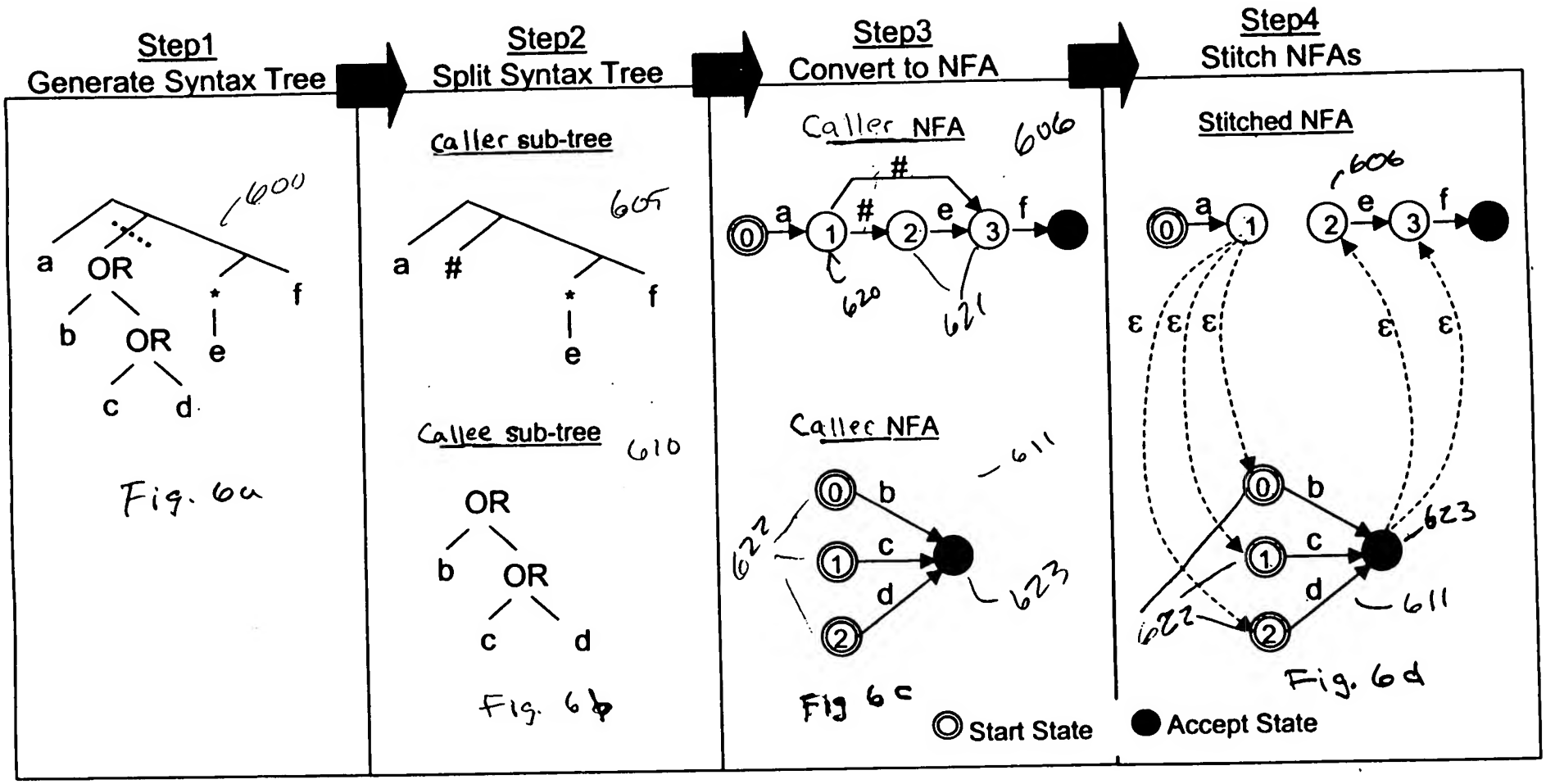


Fig. 6a

Fig. 6b

Fig 6c

Fig. 6d

Fig. 6

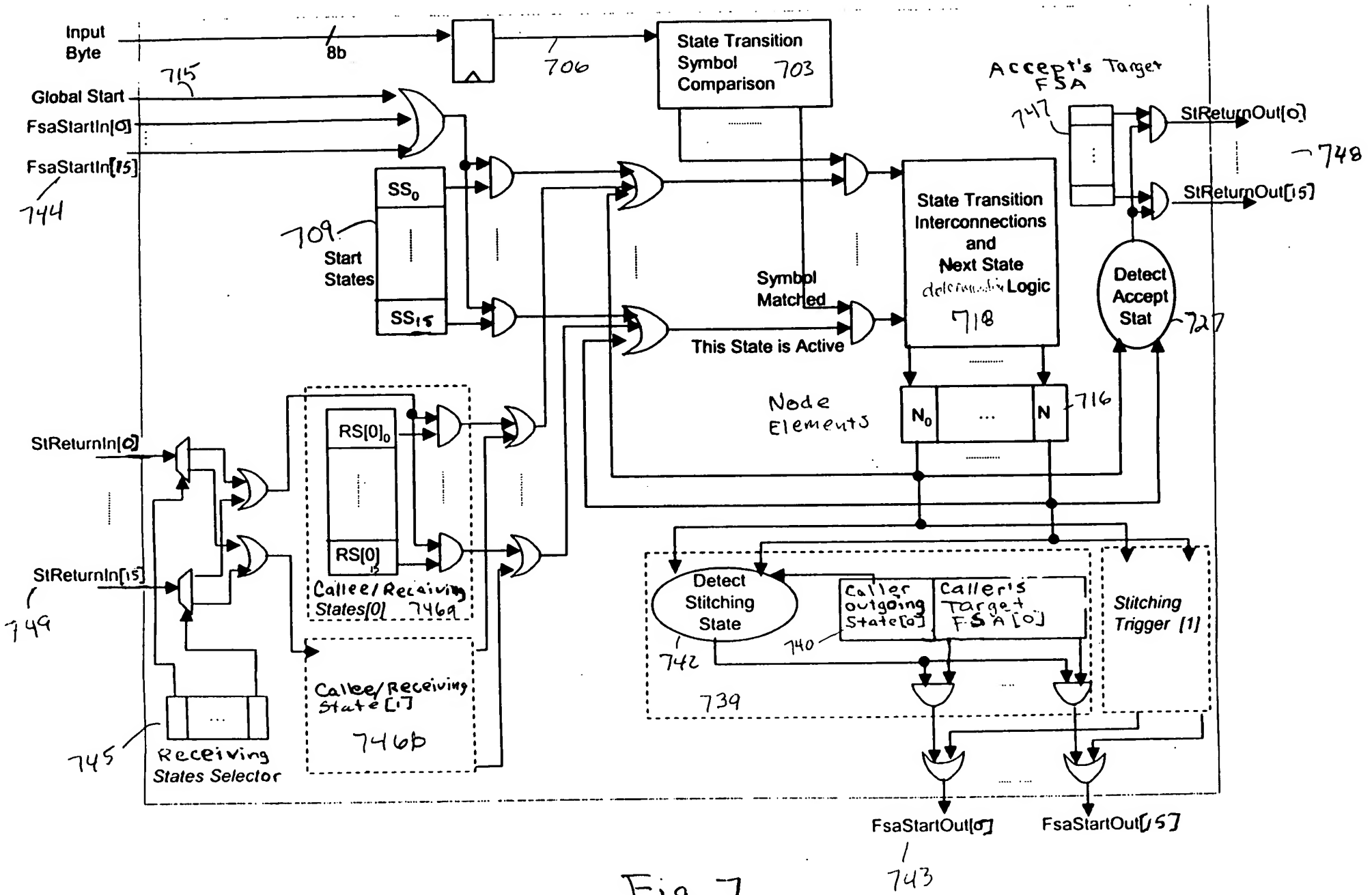

Input Byte
8b
706
State Transition Symbol Comparison 703
Accept's Target FSA
747
StReturnOut[0]
StReturnOut[15]
748
Global Start
FsaStartIn[0]
FsaStartIn[15]
744
715
SS0
SS15
709
Start States
Symbol Matched
This State is Active
State Transition Interconnections and Next State deterministic Logic
718
Detect Accept Stat
727
Node Elements
N0
N
716
StReturnIn[0]
StReturnIn[15]
749
RS[0]0
RS[0]15
Callee/Receiving States[0] 746a
Callee/Receiving State[1]
746b
745
Receiving States Selector
Detect Stitching State
742
Caller outgoing State[0]
Caller's Target FSA[0]
740
Stitching Trigger [1]
739
FsaStartOut[0]
FsaStartOut[15]
743

Fig. 7

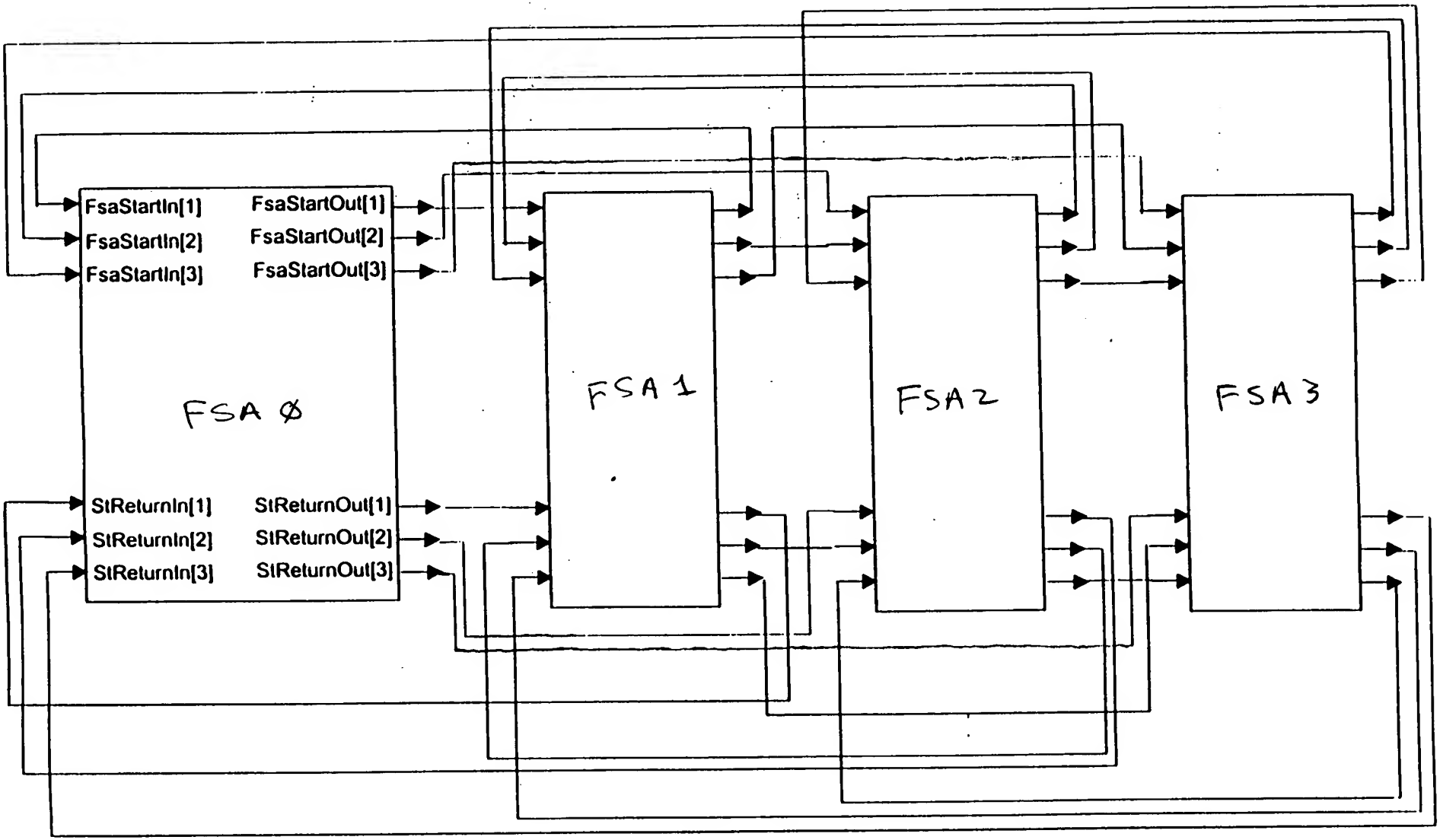

FsaStartIn[1]
FsaStartIn[2]
FsaStartIn[3]
FsaStartOut[1]
FsaStartOut[2]
FsaStartOut[3]
FSA Ø
FSA 1
FSA 2
FSA 3
StReturnIn[1]
StReturnIn[2]
StReturnIn[3]
StReturnOut[1]
StReturnOut[2]
StReturnOut[3]

Fig. 8

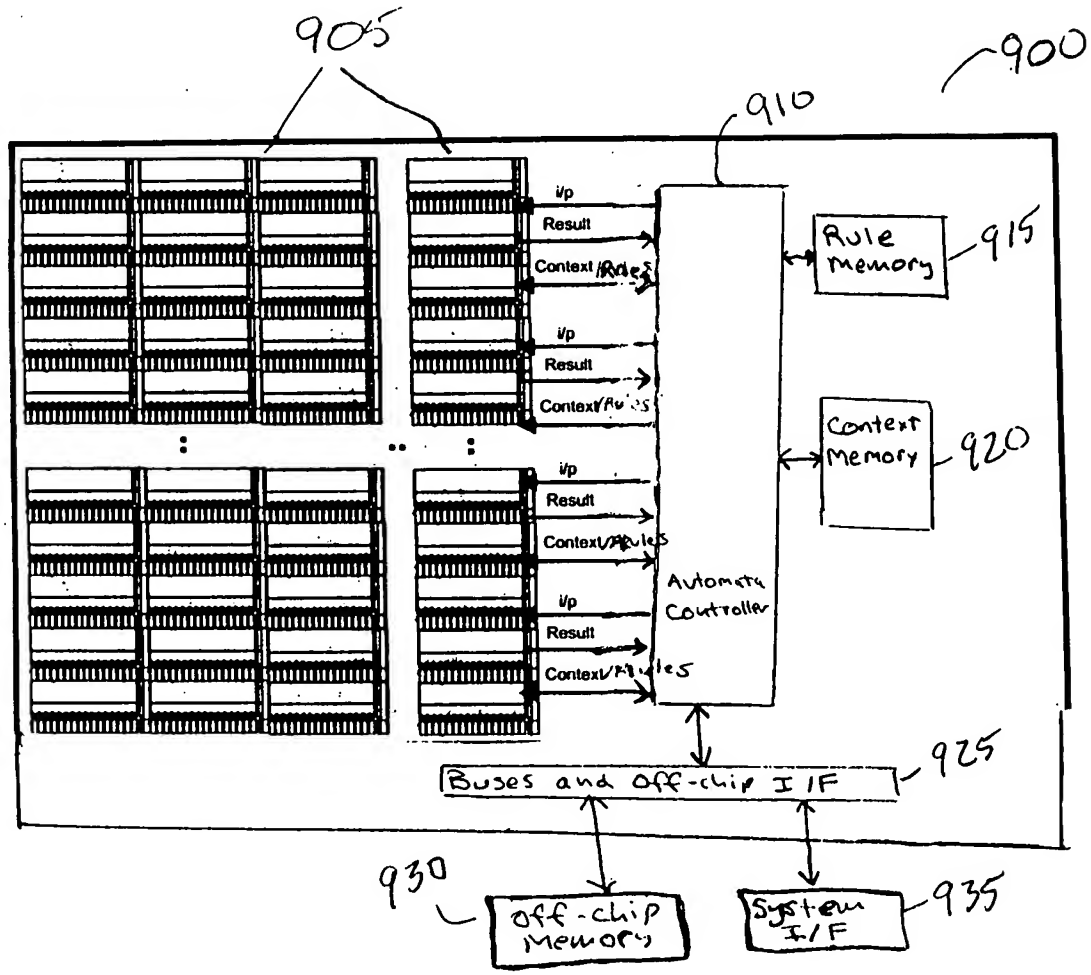

905
900
910
i/p
Result
Context/Rules
i/p
Result
Context/Rules
i/p
Result
Context/Rules
i/p
Result
Context/Rules
Automata Controller
Rule memory
915
Context Memory
920
Buses and off-chip I/F
925
930
off-chip memory
System I/F
935

Fig. 9